Introduction to Digital Logic

EECS/CSE 31L

**Assignment 4: Counter**

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**1 Block Description**

* Construct a counter that can be parameterized
* Can either increment or decrement
* Load the counter with a desired value
* Has a synchronous reset

**2 Input/Output Port Description**

|  |  |  |  |
| --- | --- | --- | --- |
| Generic Name | Data Type | Default Value | Description |
| NBIT | INTEGER | 32 | Size of counter |
| STEP | INTEGER | 1 | How much the counter increments/decrements |

|  |  |  |  |
| --- | --- | --- | --- |
| Port name | Port size | Port Type | Description |
| Clk | 1 | IN | Triggers the counting |
| Rst\_s | 1 | IN | Will reset the counter to zero when active |
| asc | 1 | IN | Increments when ‘1’ and decrements when ‘0’ |
| preload | 1 | IN | Trigger the counter to load a given value |
| din | NBIT-1 downto 0 | IN | The input value |
| dout | NBIT-1 downto 0 | OUT | The counter’s value after counting |

|  |  |  |  |
| --- | --- | --- | --- |
| Variable Name | Data Type | Port size | Description |
| count | INTEGER | NBIT-1 downto 0 | Aids in the counting process |

**3 Design Schematics**

**Truth Table:**

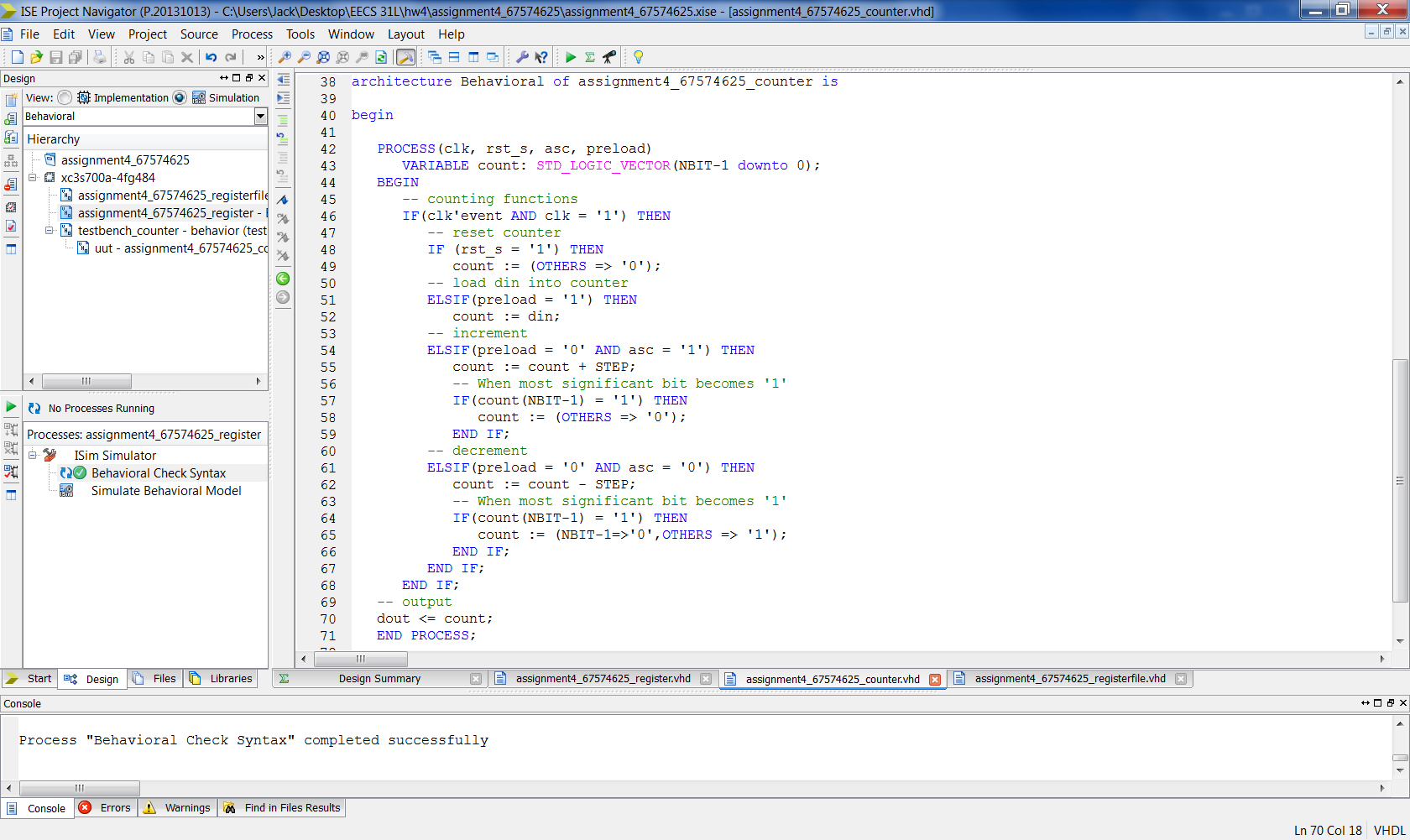
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Clk (Rising edge) | Rst\_s | asc | preload | Function |
| 1 | 1 | X | X | Reset counter to zero |
| 1 | 0 | 1 | 0 | increment |
| 1 | 0 | 0 | 0 | decrement |
| 1 | 0 | X | 1 | Load din into counter |

**Design:**

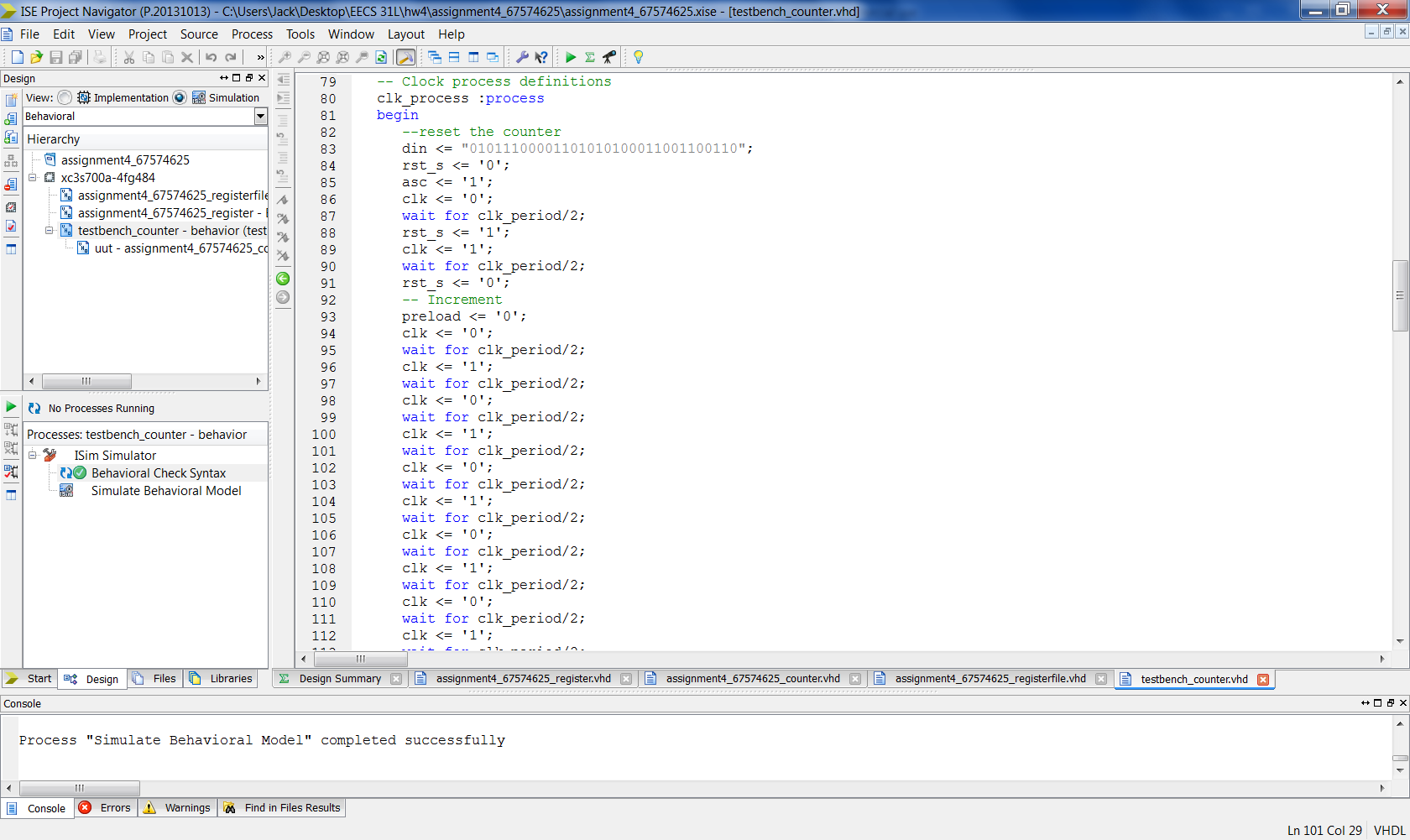


**4 Compilation**

Counter



Testbench



**5 Elaboration**

**Assumptions:**

* The counter cannot output a negative value
* The most significant bit will result in the negative value
  + Counter loops back to zero if incrementing
  + Counter loops back to the greatest positive value it can take

Regarding how I wrote my vhdl code

* I used a process with a variable called count
* Used sequential if and elsif statements

**Errors and Challenges:**

* I was having issues early on with the process statement. I didn’t realize “else if” id “elsif” in VHDL
* Misusing assignment operators; tried using signal assignment operator on a variable

**Simulation Log:**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_beh.prj} work.testbench\_counter {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_beh.prj work.testbench\_counter

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/assignment4\_67574625\_counter.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling package std\_logic\_arith

Compiling package std\_logic\_unsigned

Compiling package numeric\_std

Compiling architecture behavioral of entity assignment4\_67574625\_counter [\assignment4\_67574625\_counter(32...]

Compiling architecture behavior of entity testbench\_counter

Time Resolution for simulation is 1ps.

Compiled 8 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_isim\_beh.exe

Fuse Memory Usage: 37152 KB

Fuse CPU Usage: 561 ms

Launching ISim simulation engine GUI...

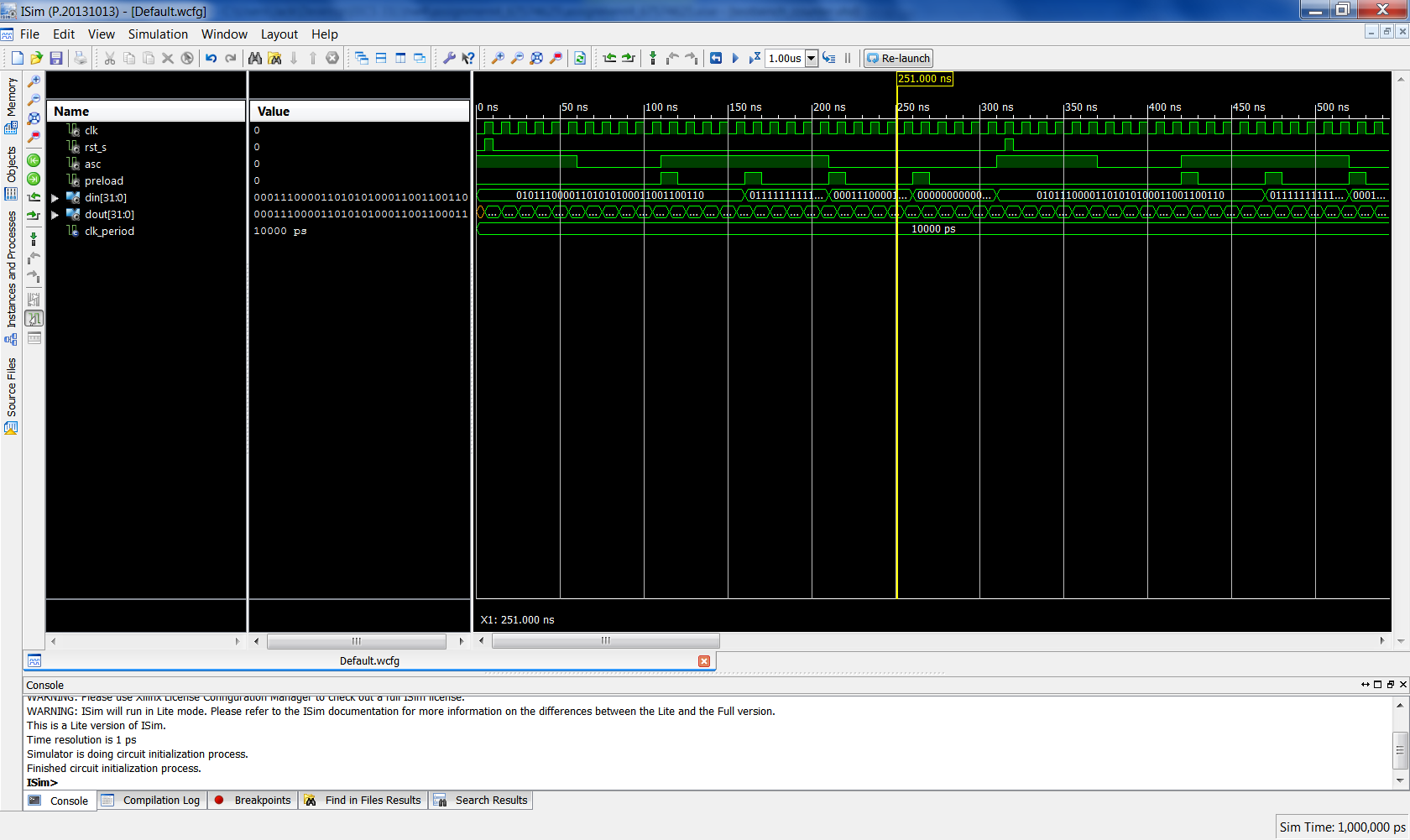
"C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_counter\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

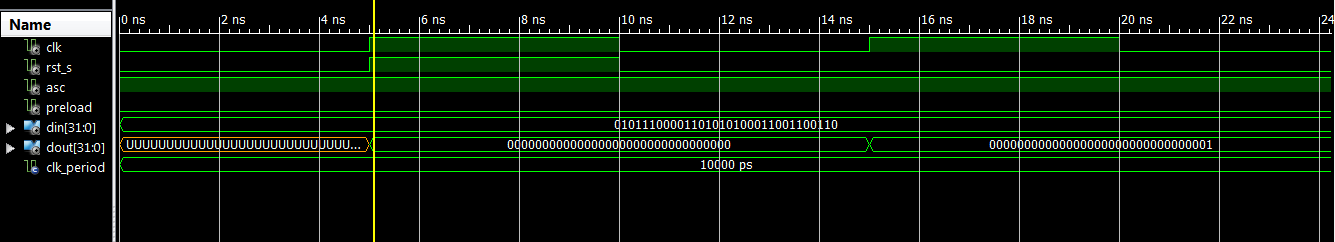
**6 Waveforms**

*Full Waveform Snapshot*

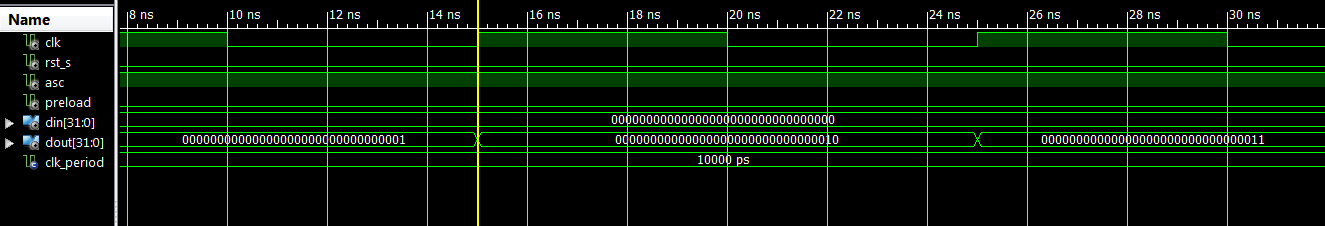


*Snapshots of Waveform*

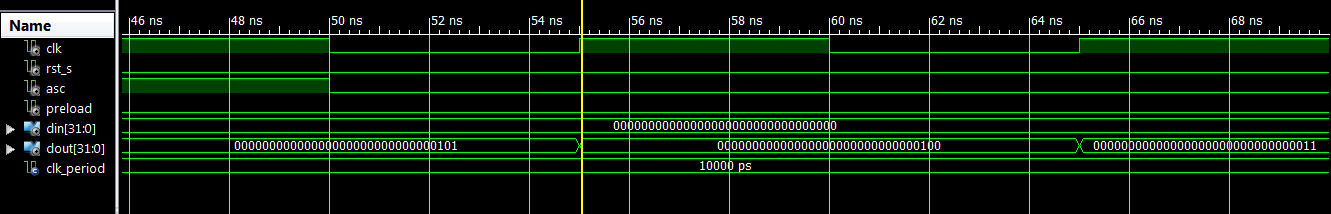
Reset Counter



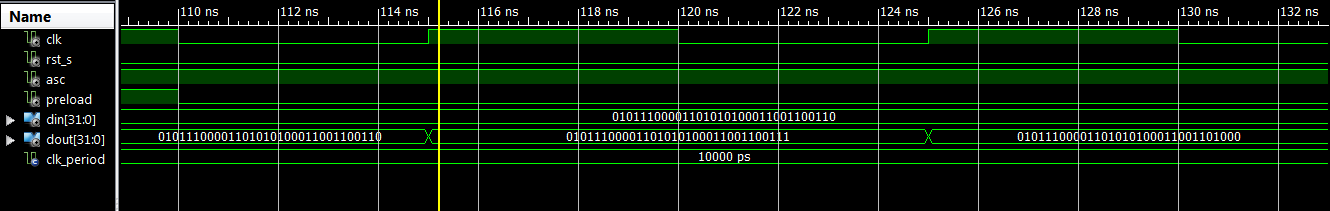
Increment



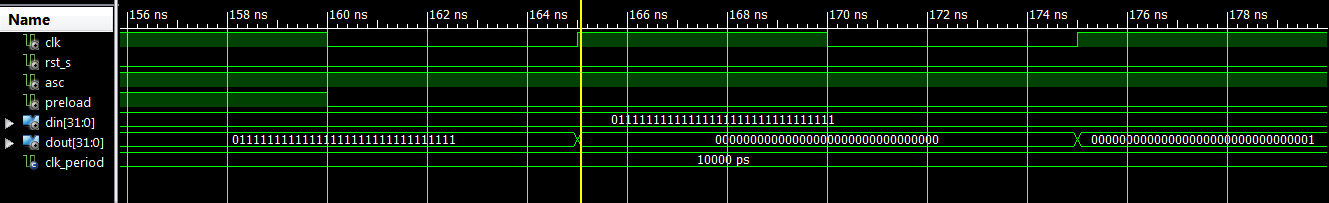
Decrement



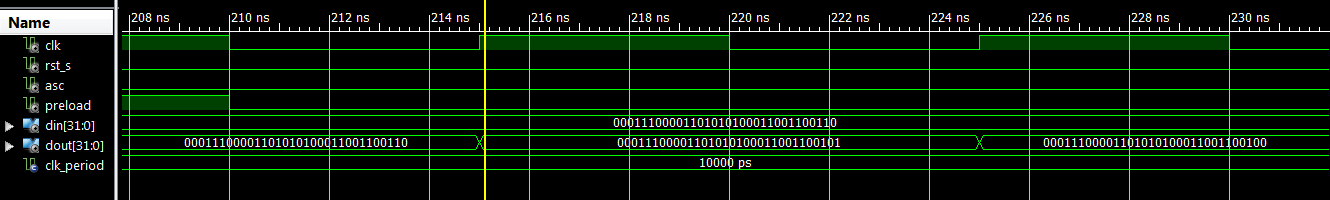
Load random value and start Incrementing



Load greatest positive value and loop back to zero and continue incrementing



Load random value and start Decrementing



Load zero and loop back to greatest positive value and continue decrementing

